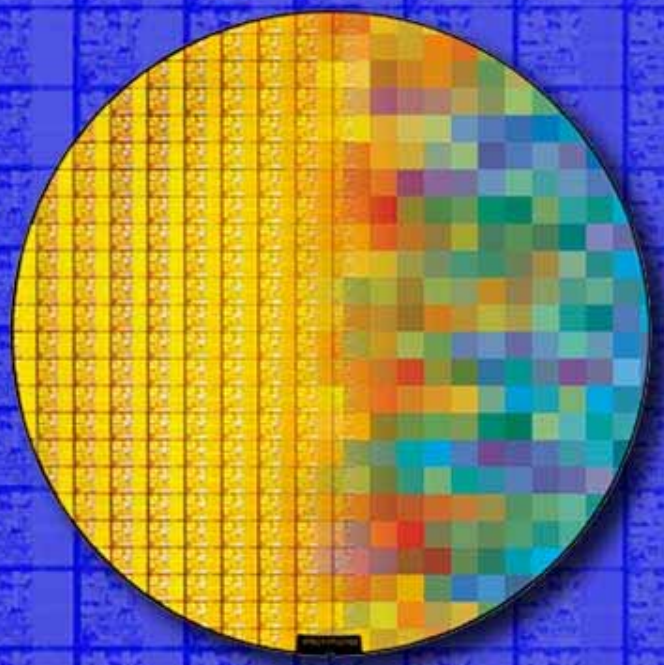


Dual Core Architecture

Benson Inkley
Senior Processor Applications Engineer

intel

Intel Developer FORUM

Objectives

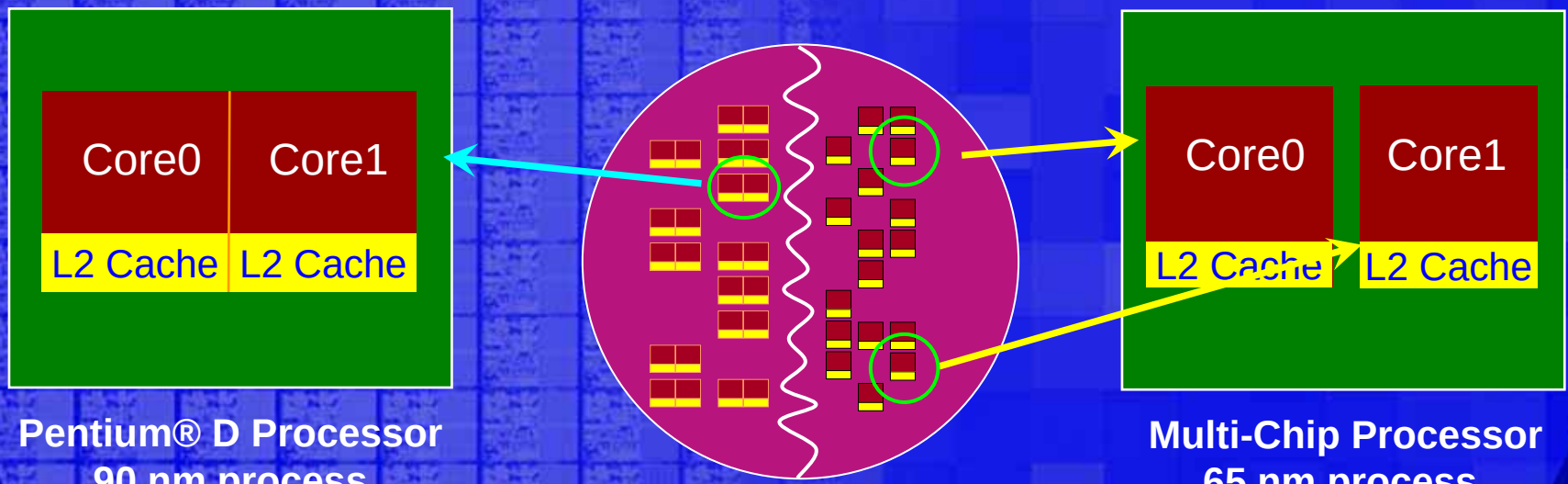
- Explain dual core concepts and implementations
- Compare Hyper-Threading (HT) Technology and dual core operation
- Review performance simulations

Agenda

- Dual core overview
- Processor Block Diagrams and Bus Interface
- HT compared to dual core
- Operating systems and application software
- Thermals and power management
- Dual core performance
- Summary

What is Dual Core

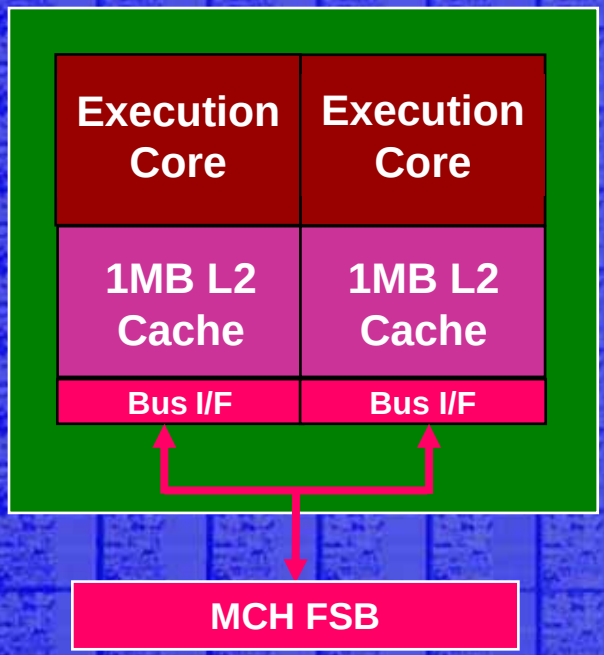
- Two independent execution cores in the same processor
- Specific implementations will vary over time
  - Driven by design efficiencies and optimizations
  - No change to OEM designs or End User experience



Pentium® D Processor
90 nm process

Multi-Chip Processor
65 nm process

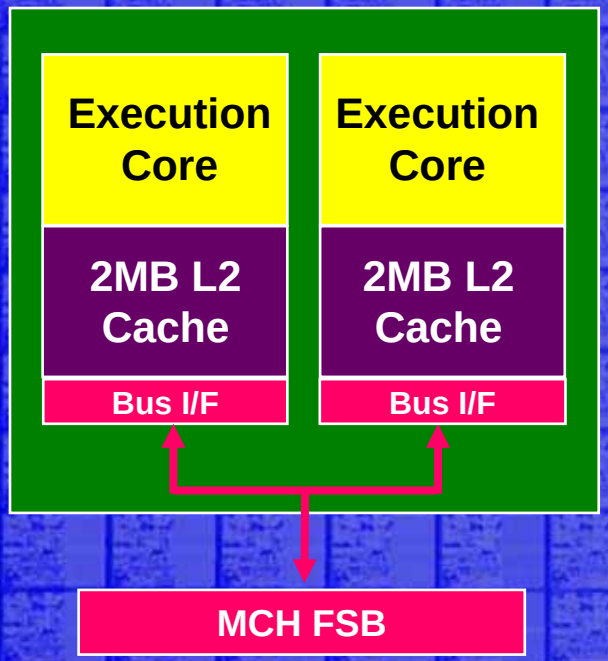
Intel® Pentium® D Processor Overview



Intel Pentium D Feature Summary	
Bus Speed	800MHz
L2 Cache	2 x 1MB
Process technology	90nm
Intel® EM64T	Yes
Execute Disable Bit	Yes
Socket	LGA 775
Availability Target	2Q'05

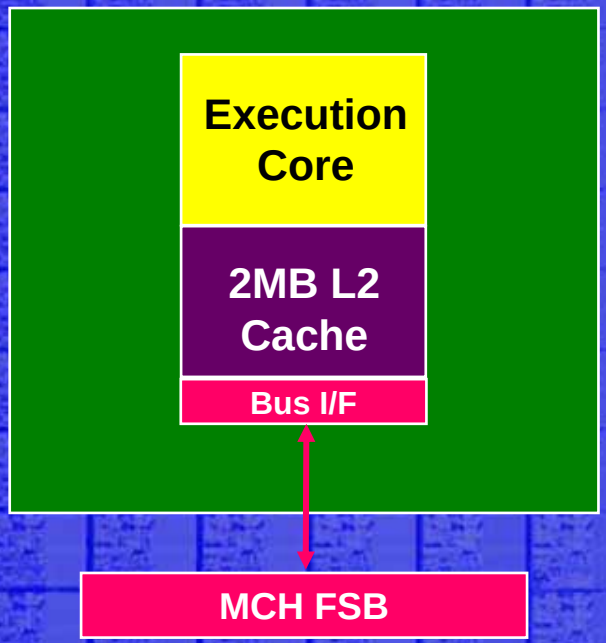
- Note: The dual core Intel® Pentium® Processor Extreme Edition supports HT Technology
  - Provides four execution threads
  - Each core runs at 3.20 GHz

Presler Processor Overview



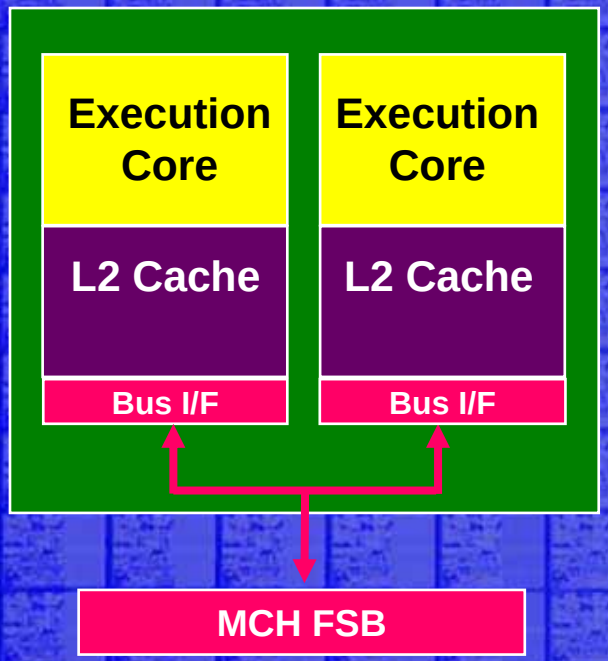
Presler Feature Summary	
Process technology	65nm
Intel® EM64T	Yes
Execute Disable Bit	Yes
Socket	LGA 775
Availability Target	1H'06

Cedar Mill Processor Overview



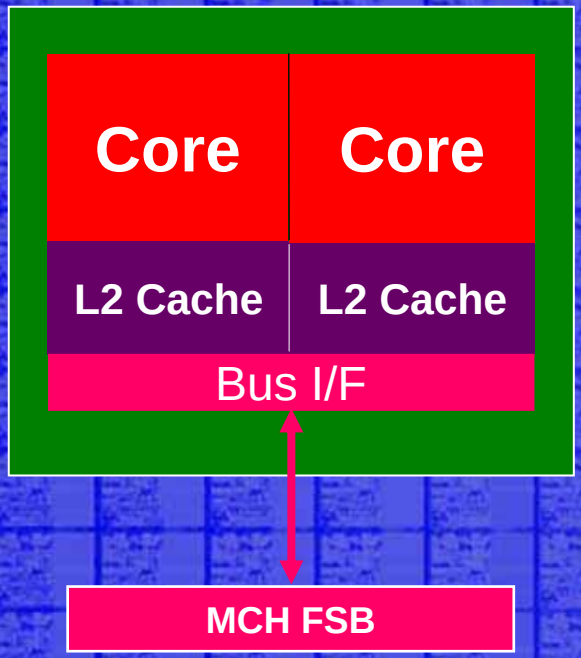
Cedar Mill Feature Summary	
Process technology	65nm
Supports HT	Yes
Intel® EM64T	Yes
Execute Disable Bit	Yes
Socket	LGA 775
Availability Target	1H'06

DP Dempsey Processor Overview



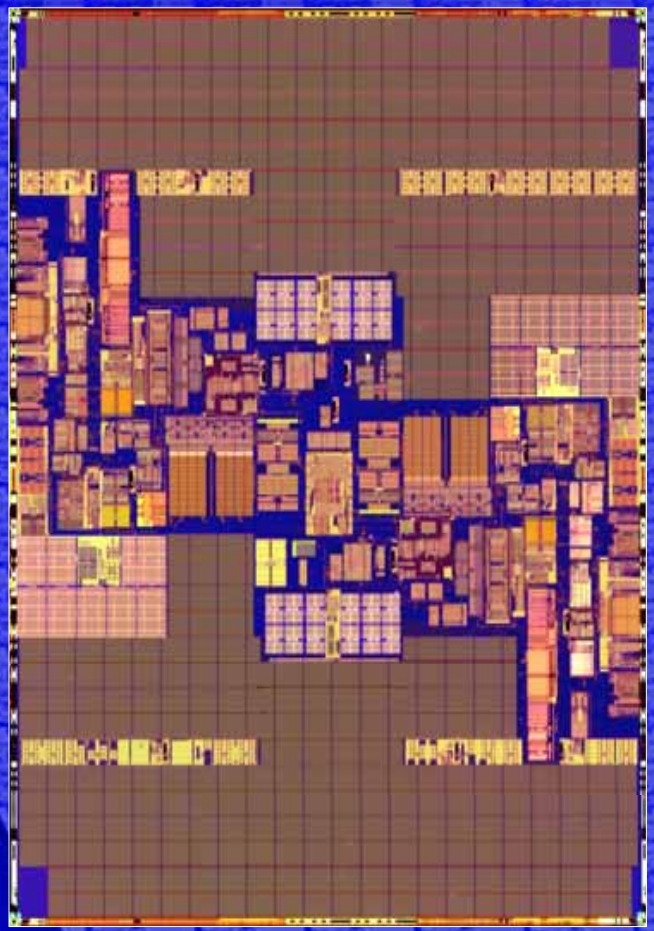
DP Dempsey Feature Summary	
Process technology	65nm
Hyper-Threading Technology	Yes
Intel® EM64T	Yes
Execute Disable Bit	Yes
Socket	LGA 771
Availability Target	Q1'06

MP Paxville Processor Overview



MP Paxville Feature Summary	
Process technology	90nm
Hyper-Threading Technology	Yes
Intel® EM64T	Yes
Execute Disable Bit	Yes
Availability Target	Q1'06

Itanium Dual Core: Montecito



Montecito Feature Summary	
Simultaneous Threads	4
Process technology	90nm
L2 Instruction Cache	2 x 1 MB
L3 Cache	2 x 12 MB
Transistors	1,720,000,000
Availability Target	Q4'05

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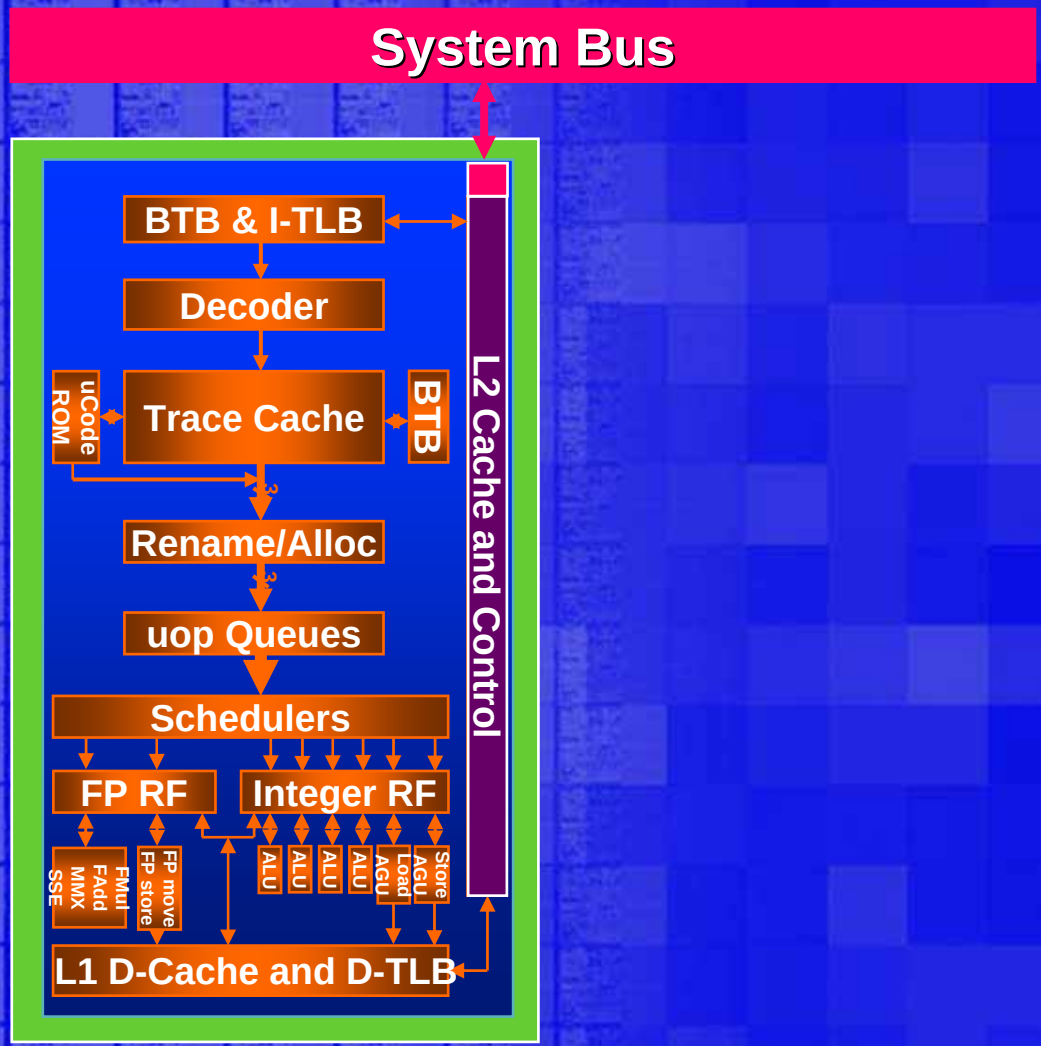
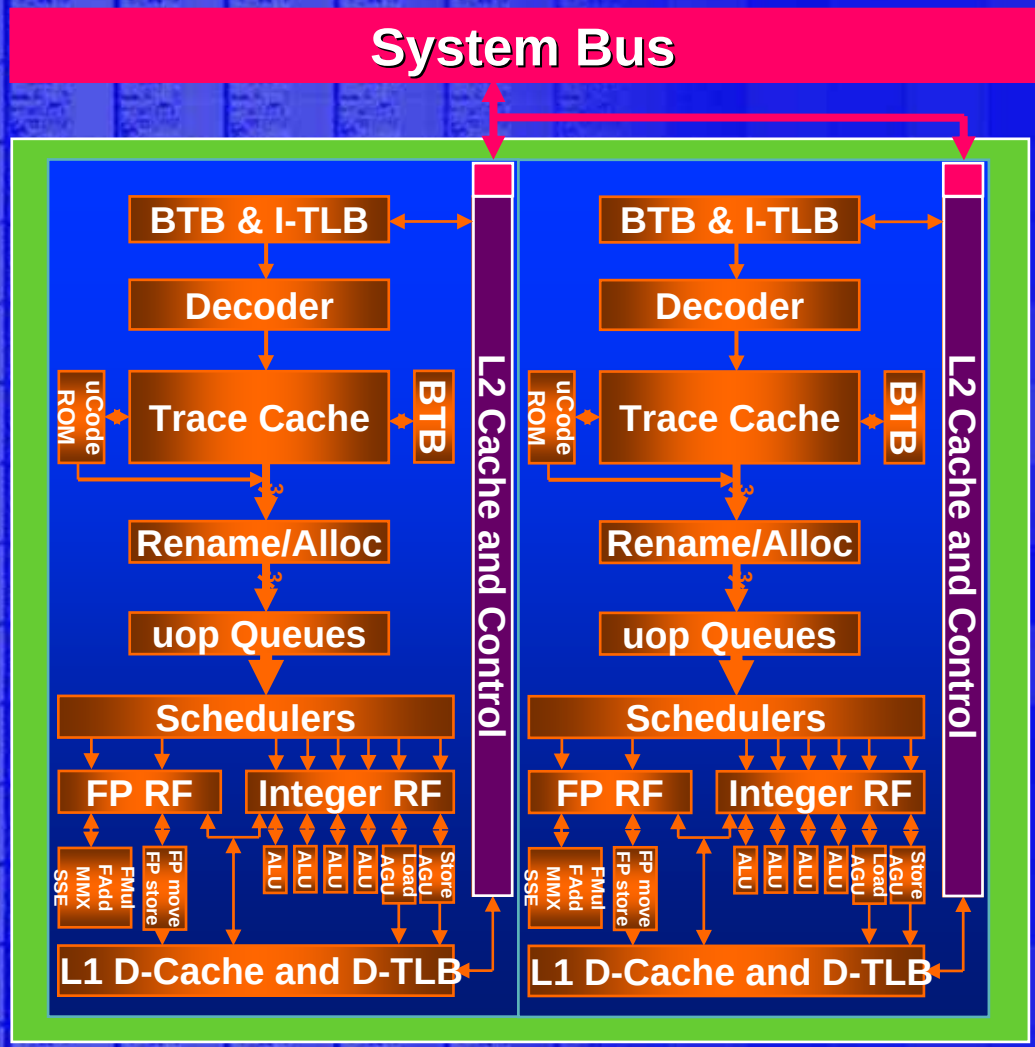
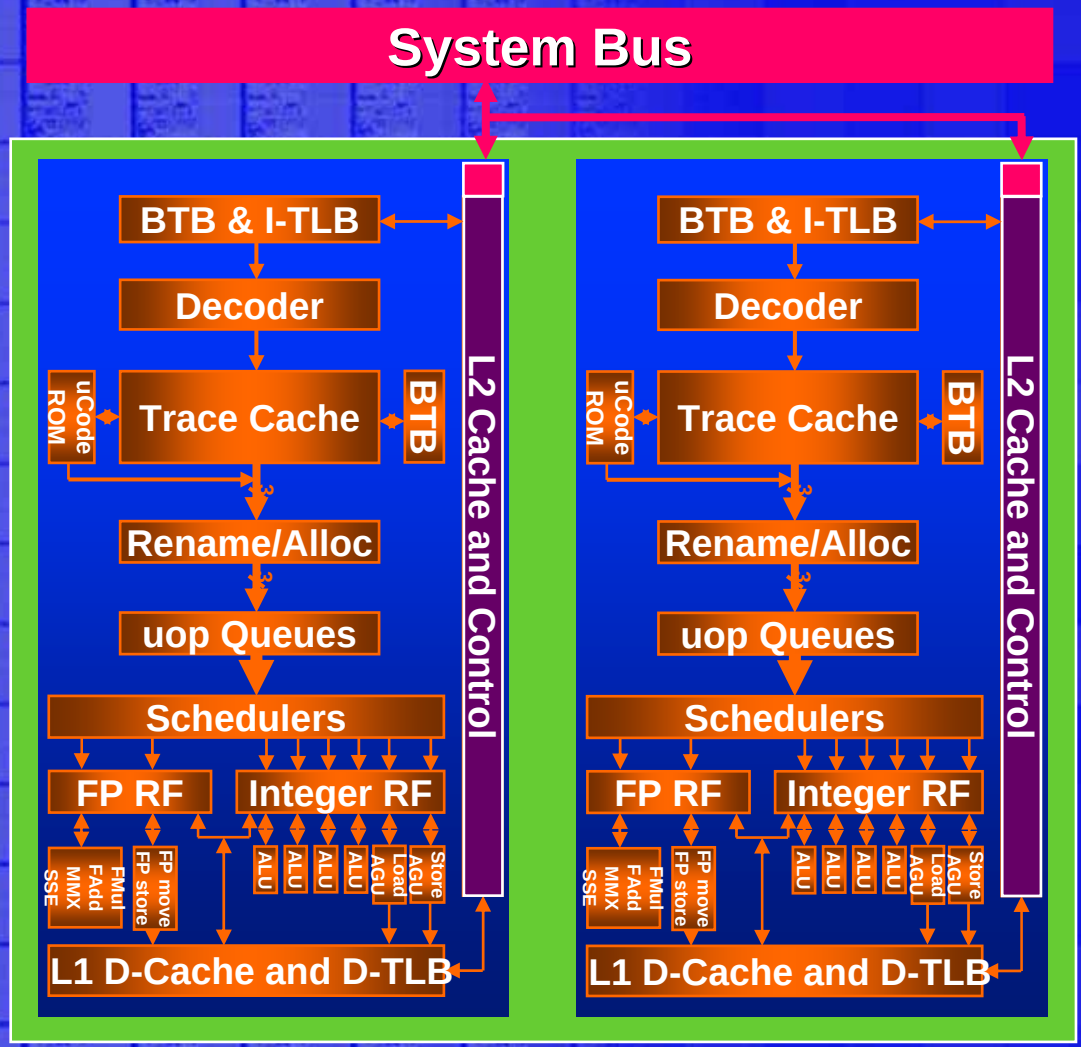
Pentium® 4 Processor Block Diagram



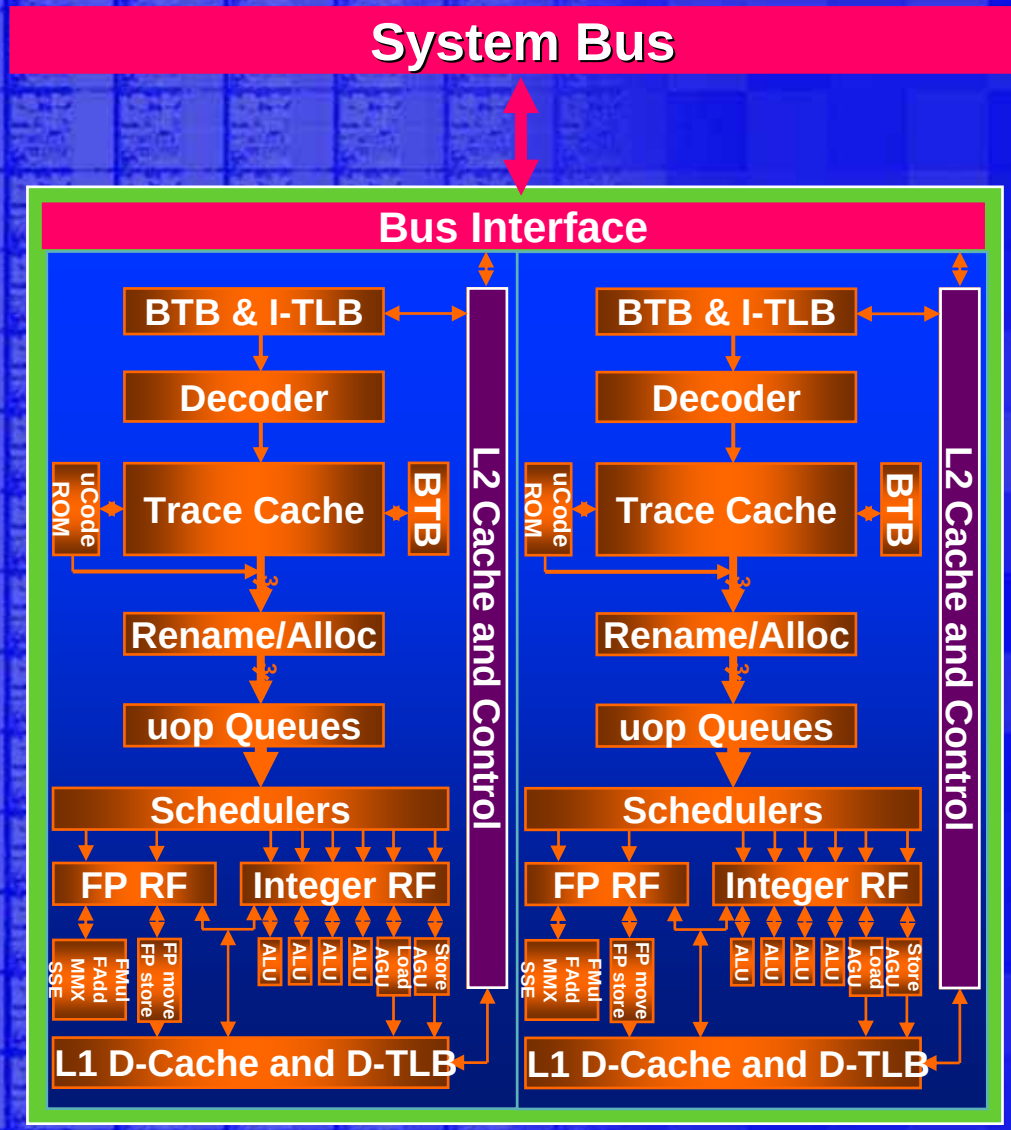
Pentium D Processor Block Diagram



Presler Block Diagram

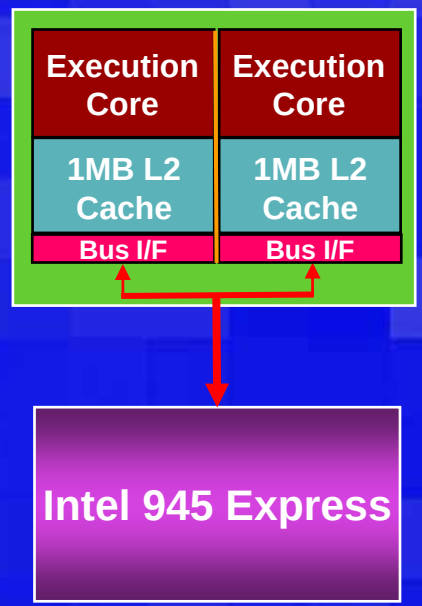


Paxville Processor Block Diagram



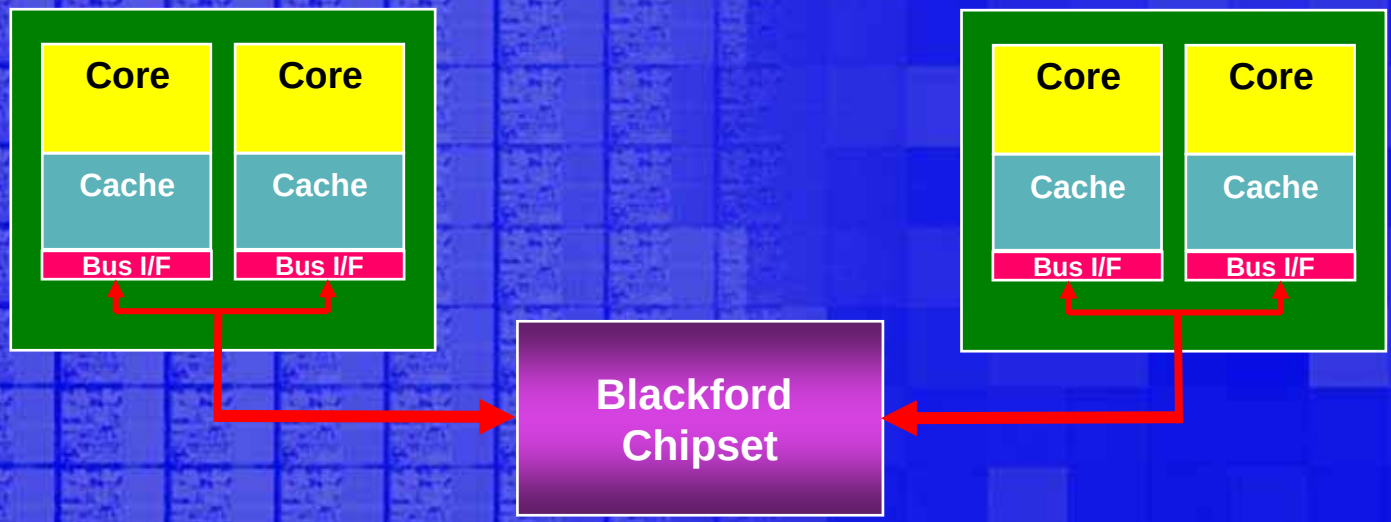
Intel 9/55945 Express Chipset Interface

- DT package defines which die is Core 0 and which is Core 1
  - Core 0 is the boot strap device (BSD)
  - BREQ lines routed the same as single core processors
- Software will recognize the difference between 0 and 1
- Dual core processors are not supported on the Intel® 925 Express Chipset or the Intel® 915 Express Chipsets
  - Processor will not boot
  - VR is shut down
  - No harm to board or processor



Dempsey Platform Bus Interface

- Chipset has two separate busses, one for each processor
- Independent busses allow more efficient data transfers



Paxville Bus Interface

- MP chipset supports up to 4 dual core processors
  - Shared driver on processor permits 2 sockets per bus
- Boot strap processor depends on configuration
  - Will change with quantity and location of processors
  - May also change in the event of a field upgrade

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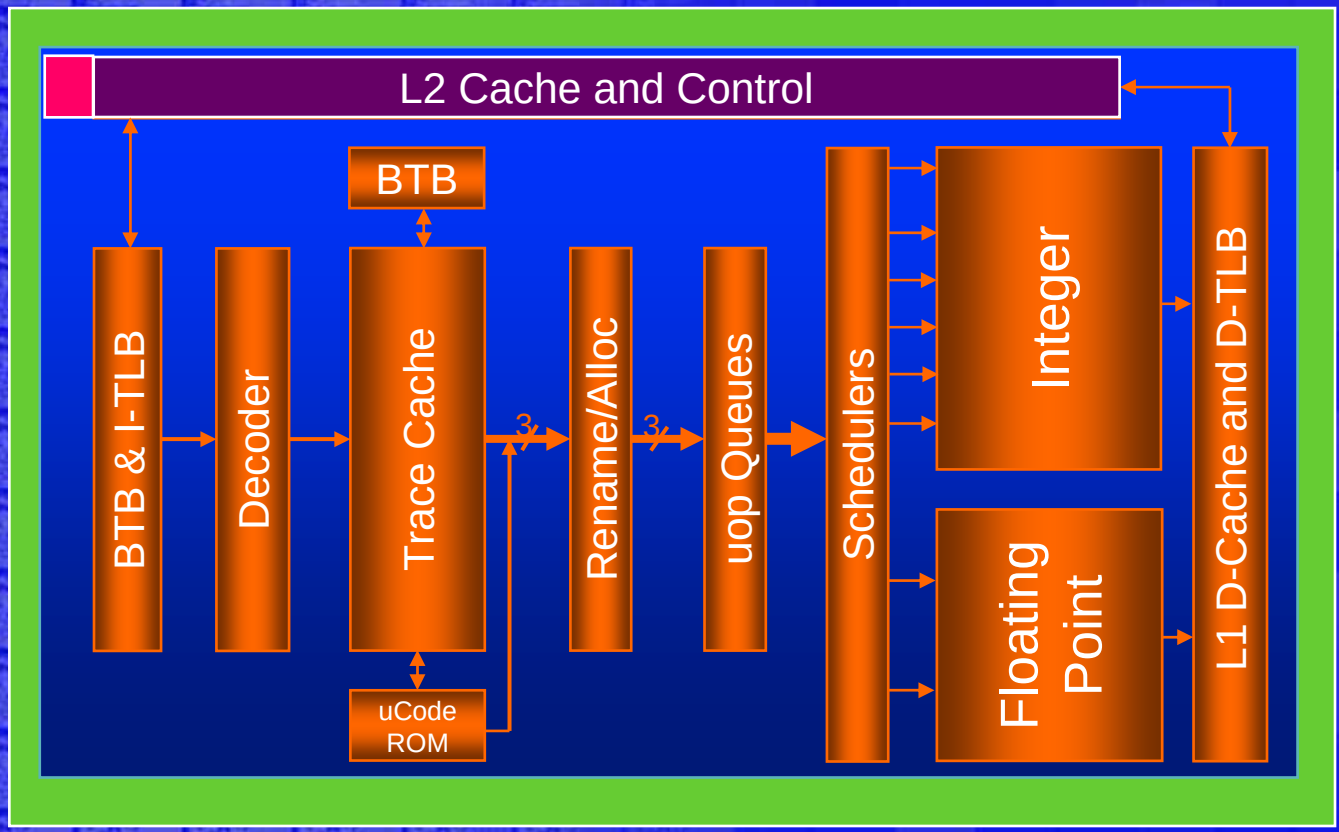
Hyper Threading and Dual Core Definitions

- HT – Hyper Threading: 2 threads running on the same execution core
  - Shares functional execution units
  - Shares cache hierarchy
- DC – Dual Core: 2 execution cores in the same processor package
  - Share only the system bus
  - Similar concept as Dual Processing
- DP/MP – Dual/Multi-Processing: 2 or more processors in the same system
  - Share only the system bus
  - Multiple sockets multiply execution resources

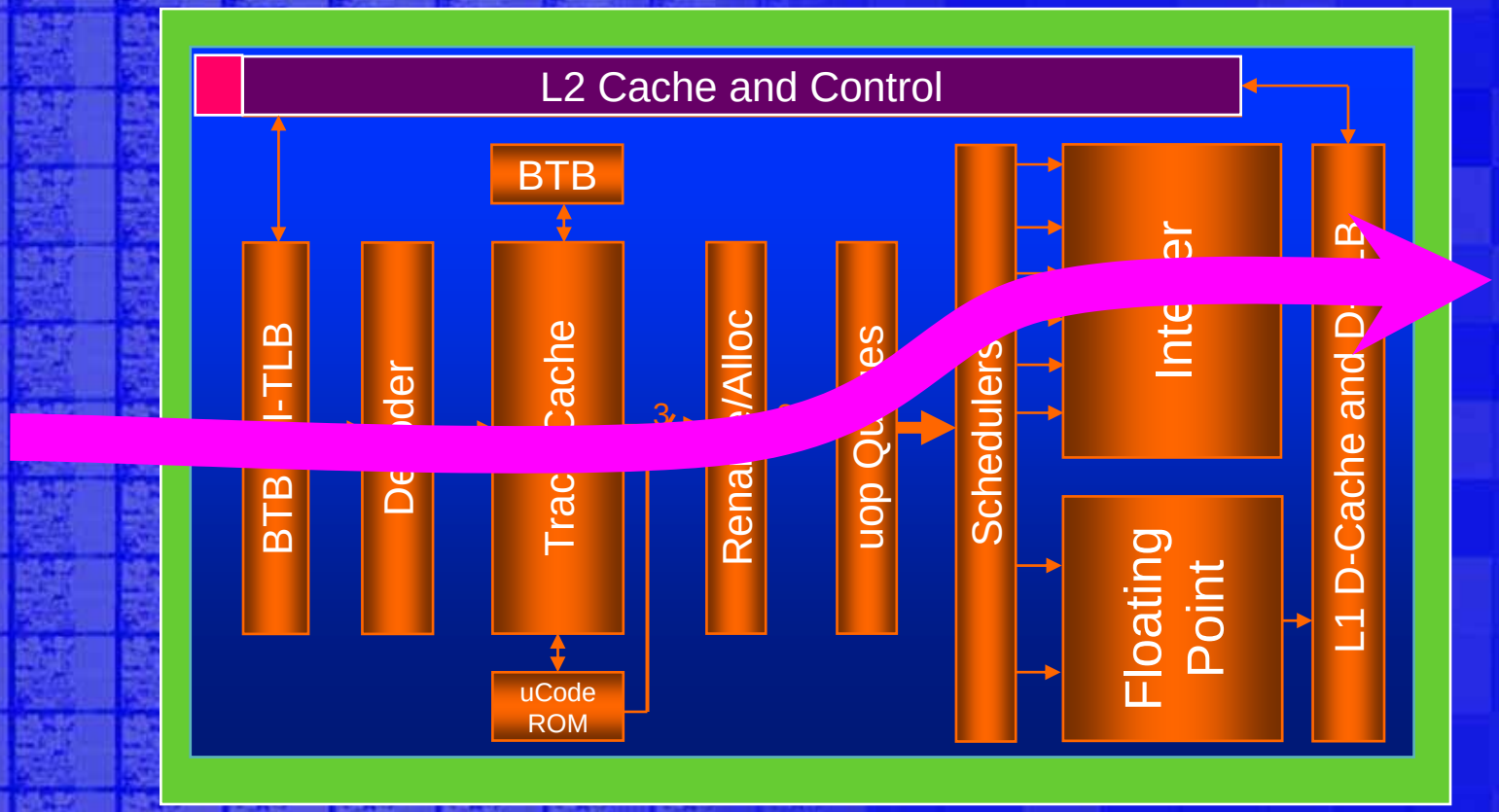
Pentium 4 Processor Without HT

Integer Thread



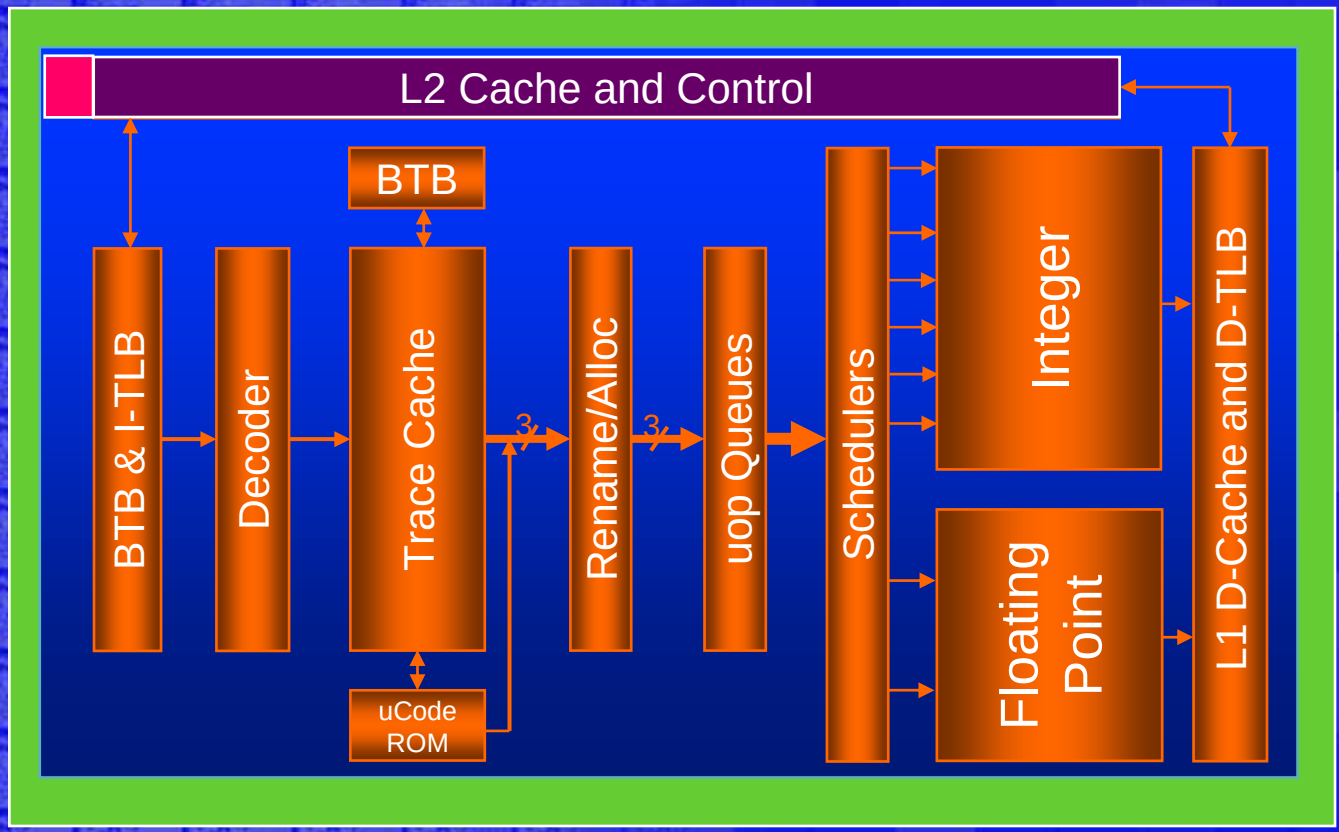
Pentium 4 Processor Without HT

Integer Thread



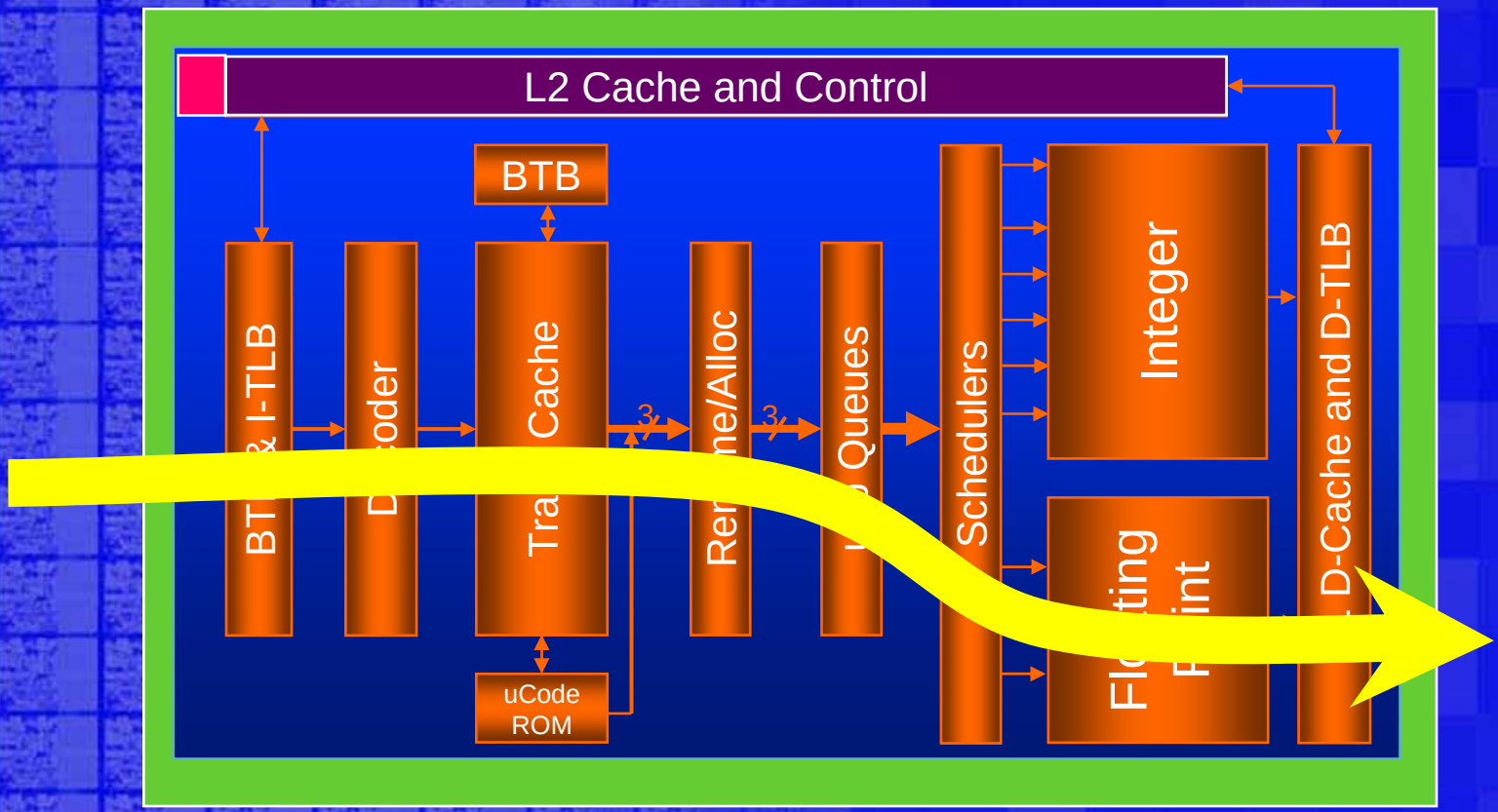
Pentium 4 Processor Without HT

Floating Point Thread



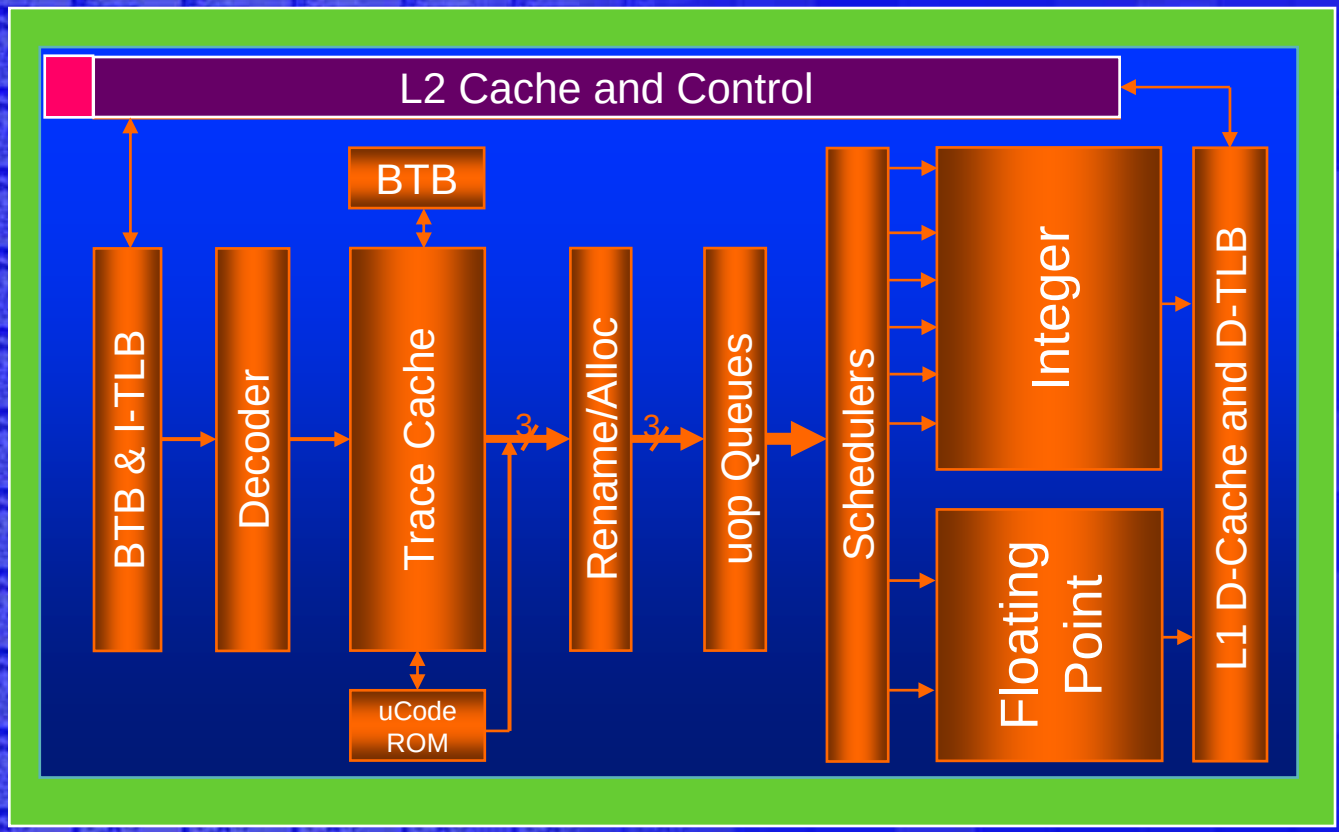
Pentium 4 Processor Without HT

Floating Point Thread



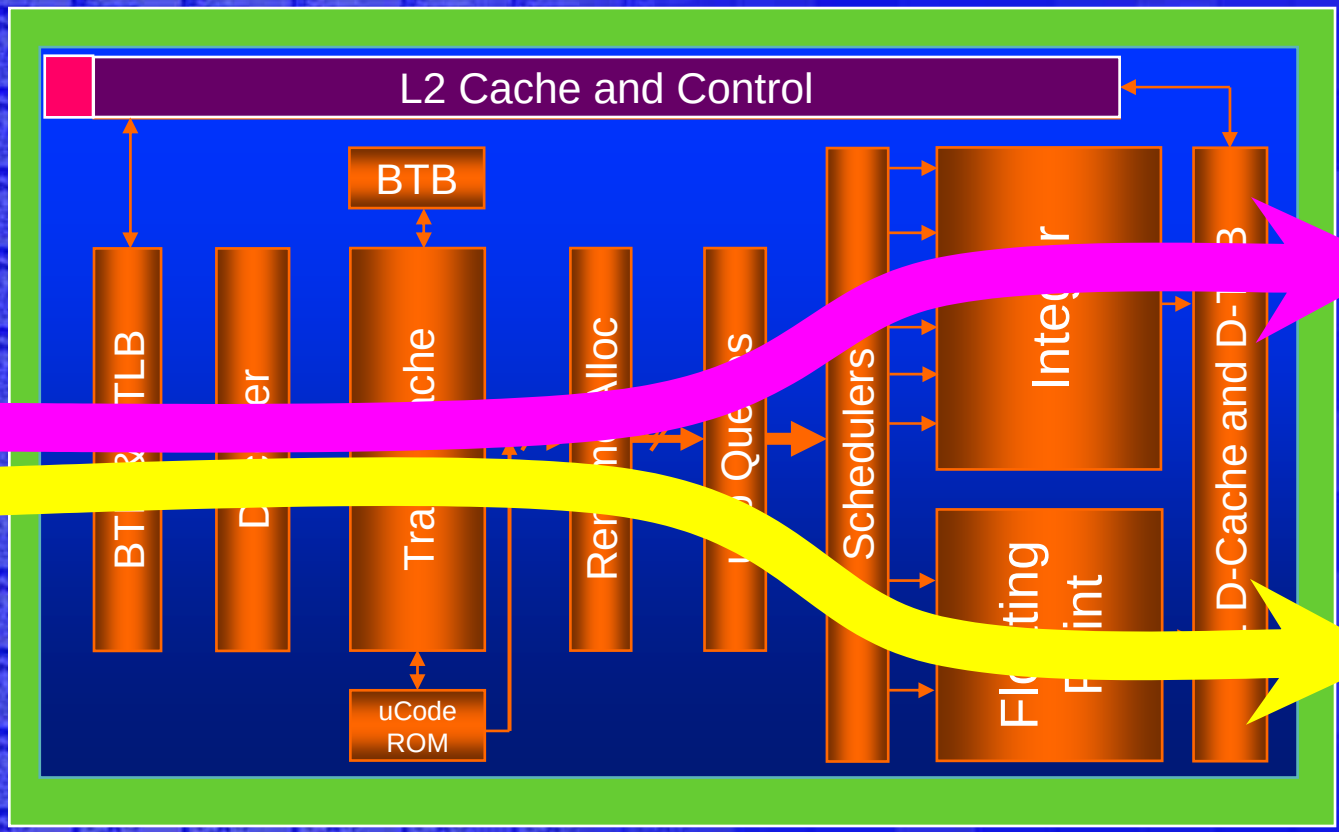
Pentium 4 Processor With HT

Integer and Floating Point Threads



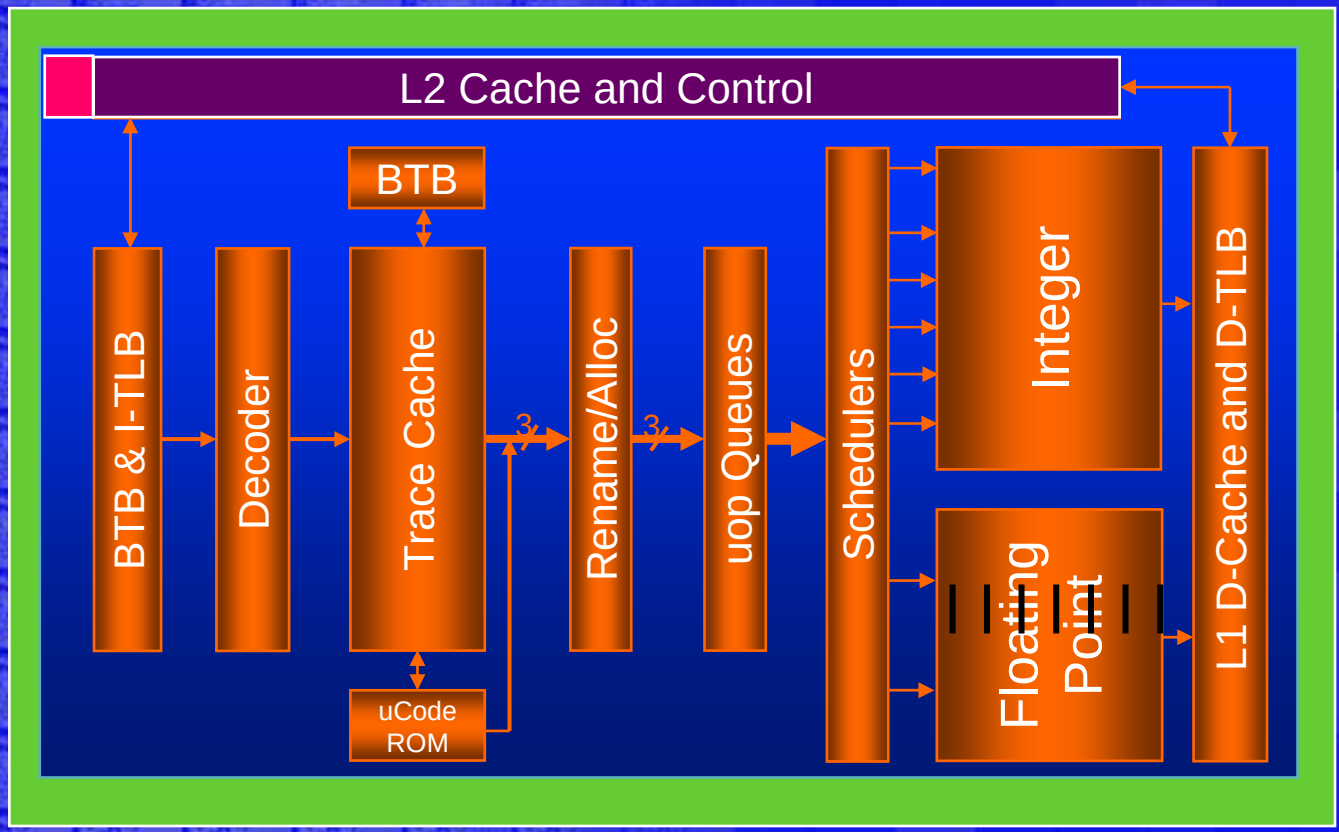
Pentium 4 Processor With HT

Integer and Floating Point Threads



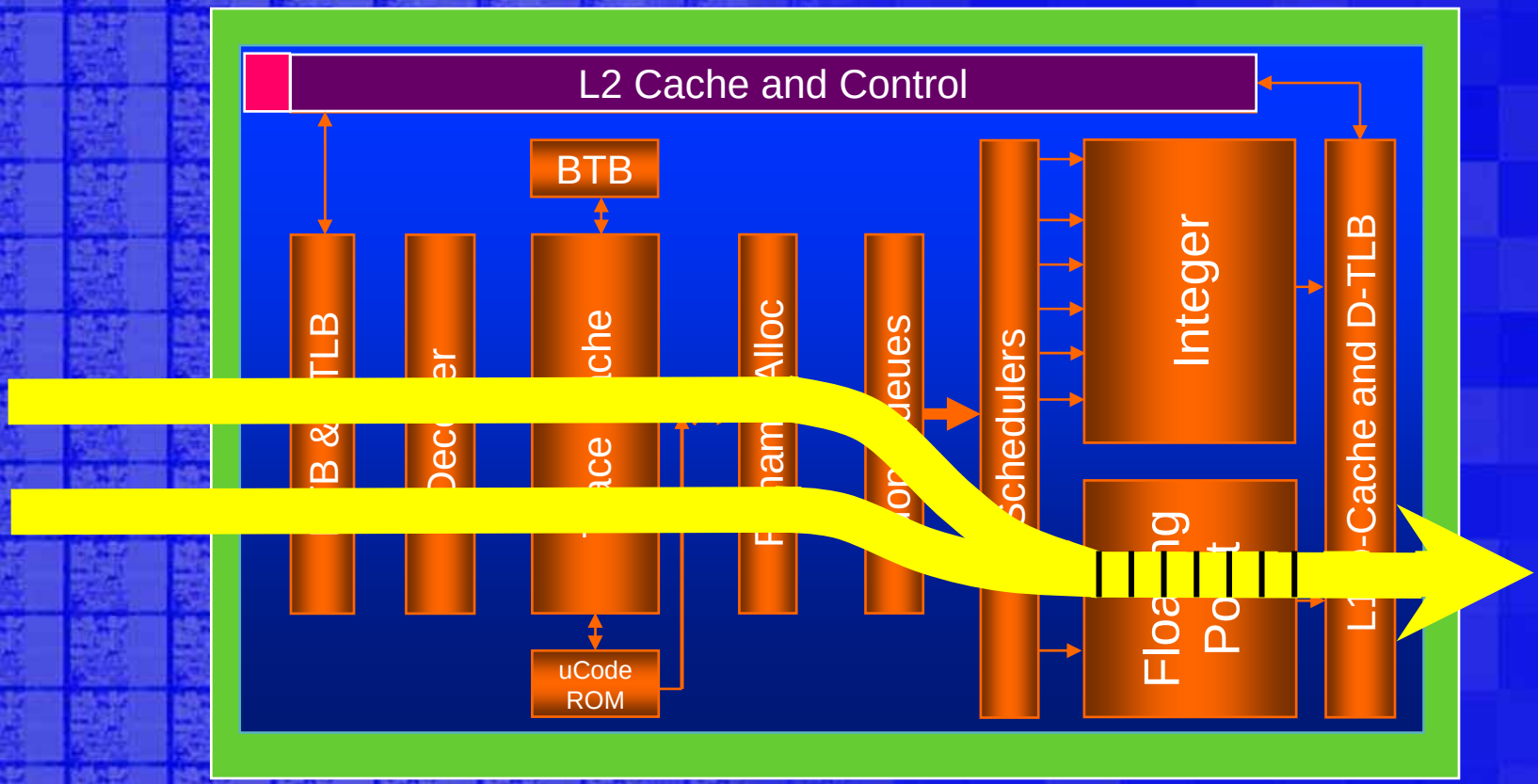
Pentium 4 Processor With HT

Two Floating Point Threads



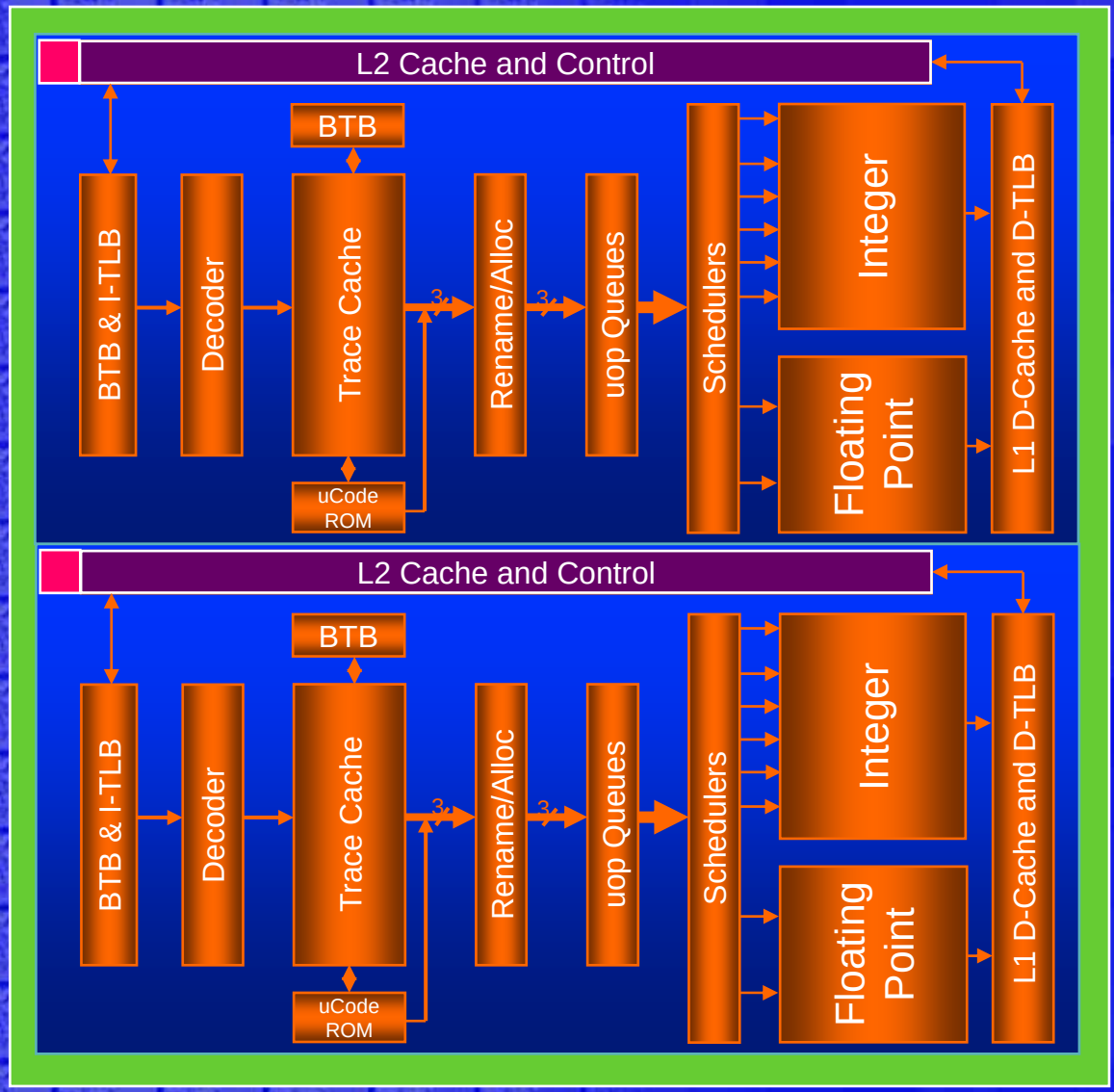
Pentium 4 Processor With HT

Two Floating Point Threads



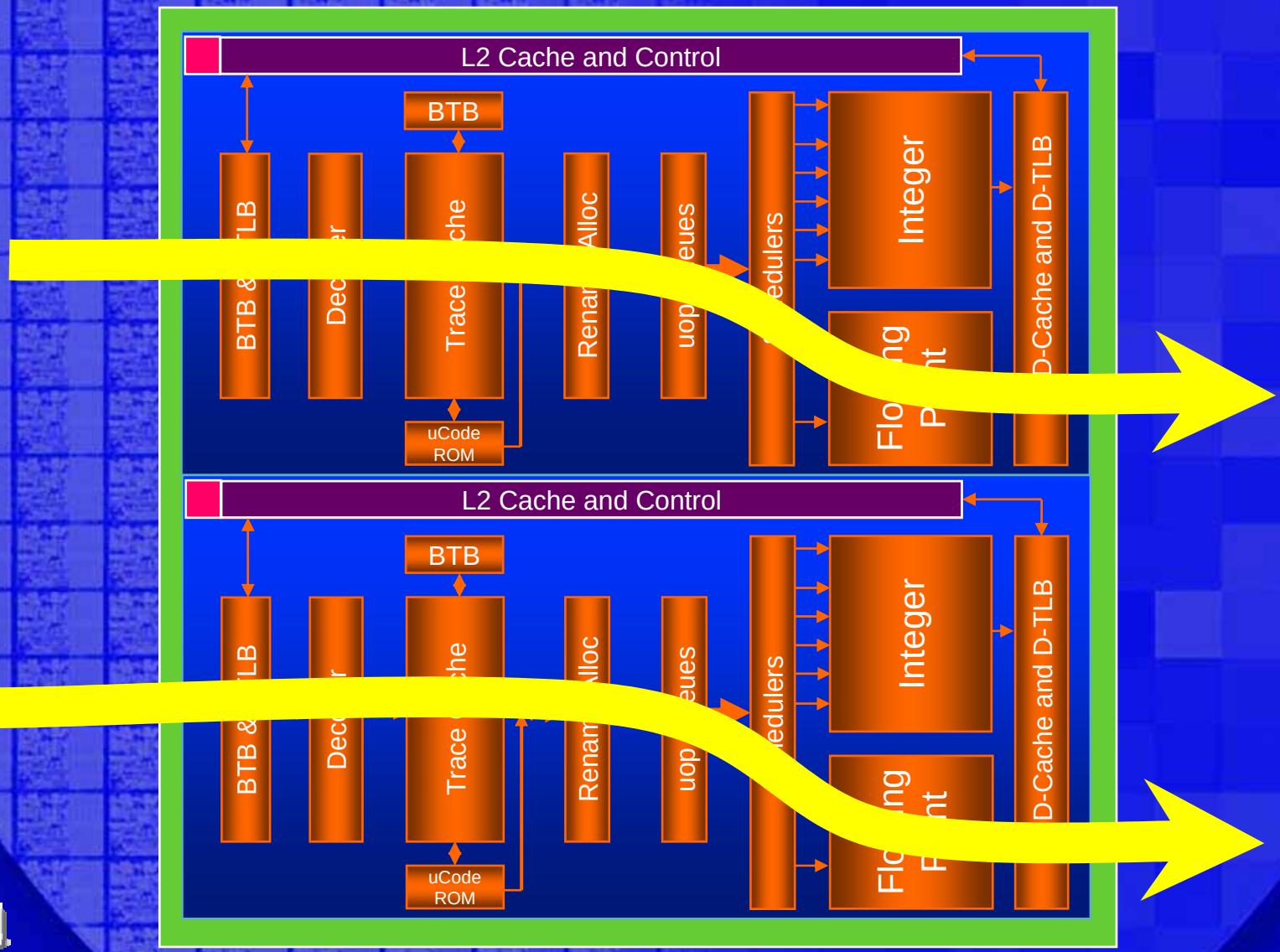
Pentium D Processor

Two Floating Point Threads



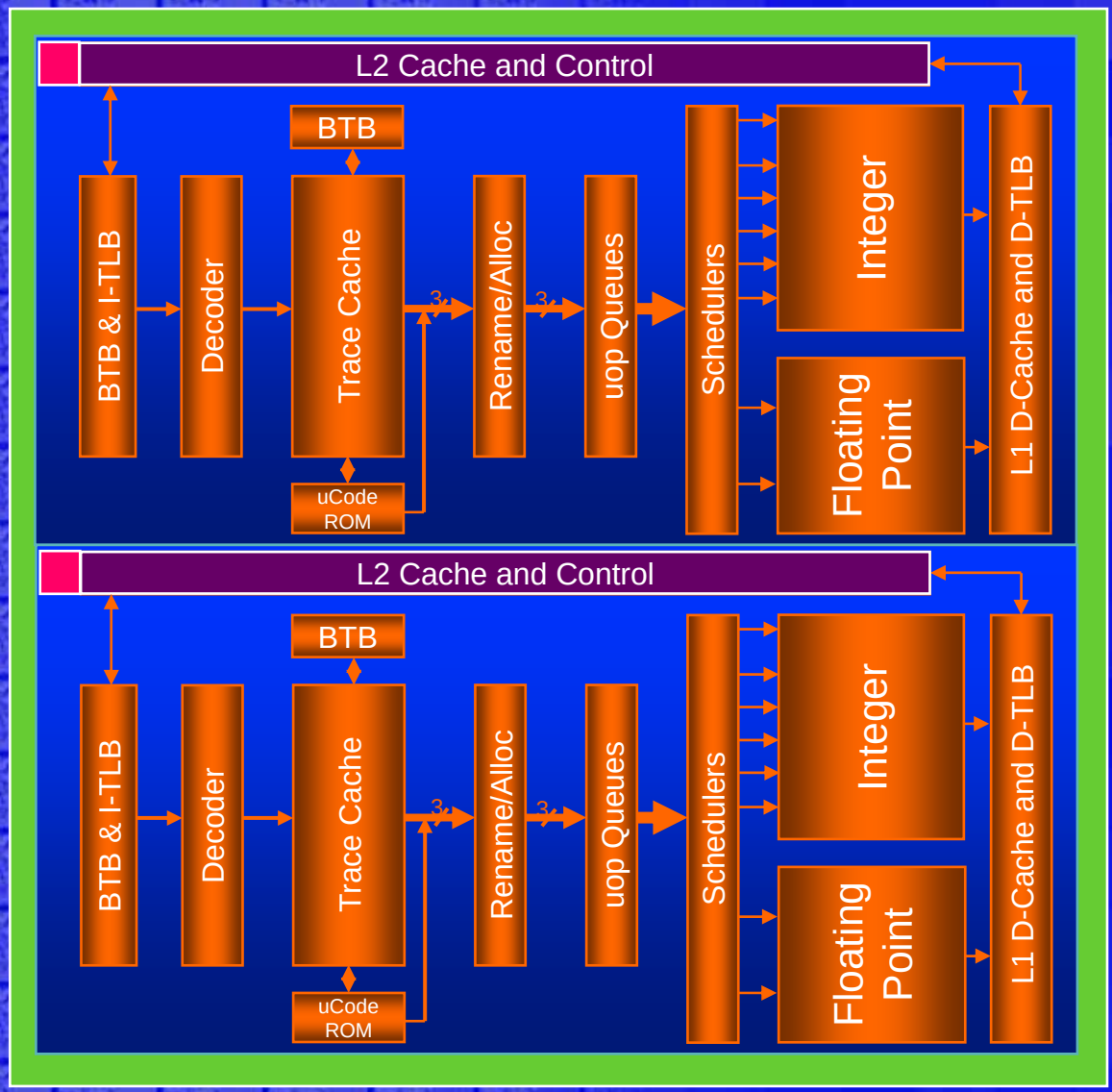
Pentium D Processor

Two Floating Point Threads



Dual Core Pentium Processor Extreme Edition

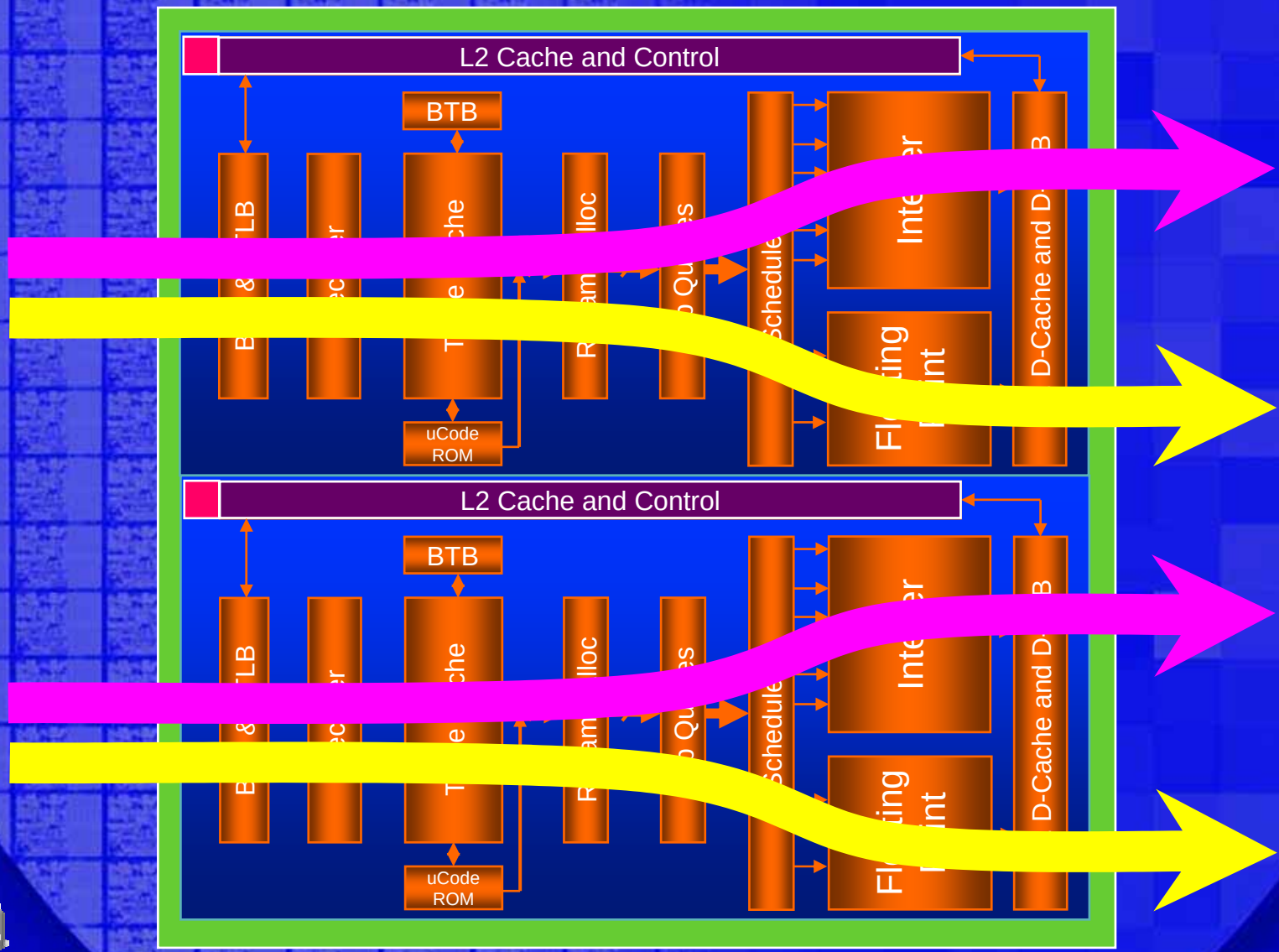
Supports HT
Multiple Integer and Floating Point Threads



Dual Core Pentium Processor Extreme Edition

Supports HT

Multiple Integer and Floating Point Threads



Agenda

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Multi-Core Software Support

- OEMs should contact OS Vendors to confirm specific support plans
  - Red Hat* and SuSe* Linux is per socket
  - Microsoft Windows* license is per socket
- OS's are already multi-threaded and support multi-core processors
- Software does not need to be re-written to run on dual core processors
- Applications that are HT enabled will benefit from the parallelism provided in dual core processors
  - By understanding how the program utilizes it's data, code can be written with threading in mind to improve performance
  - If an application is not HT optimized, then it may benefit from being rewritten
- Over 100 HT and dual core optimized client applications available today
  - Major Operating Systems
  - Video/Audio Recording/Editing
  - Games

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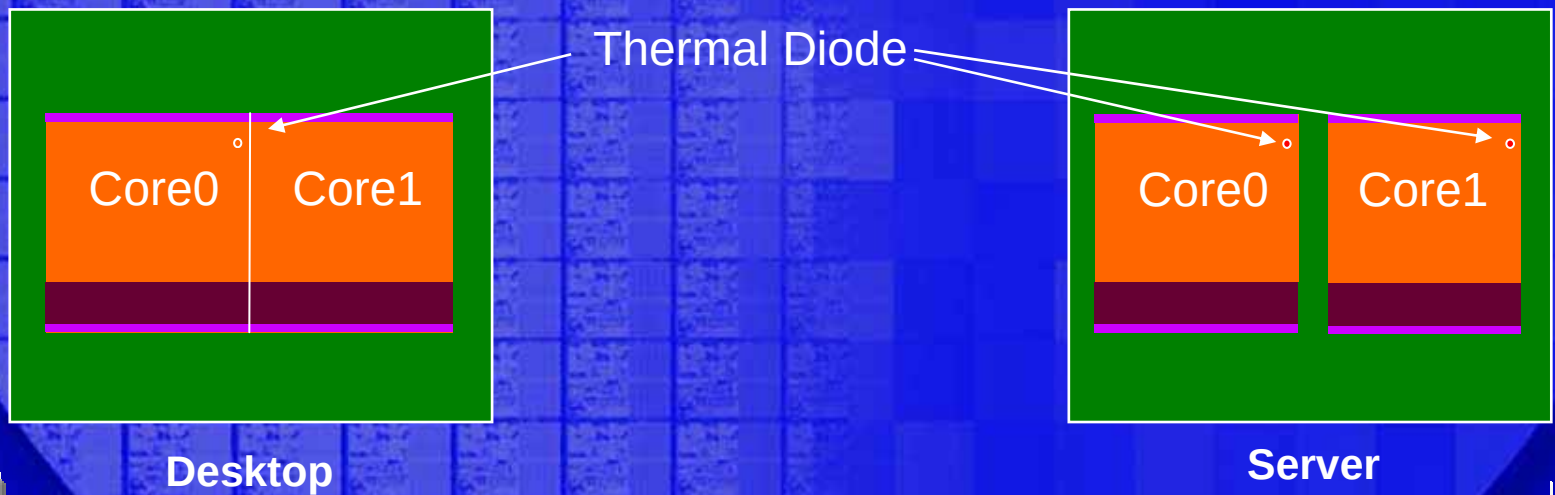
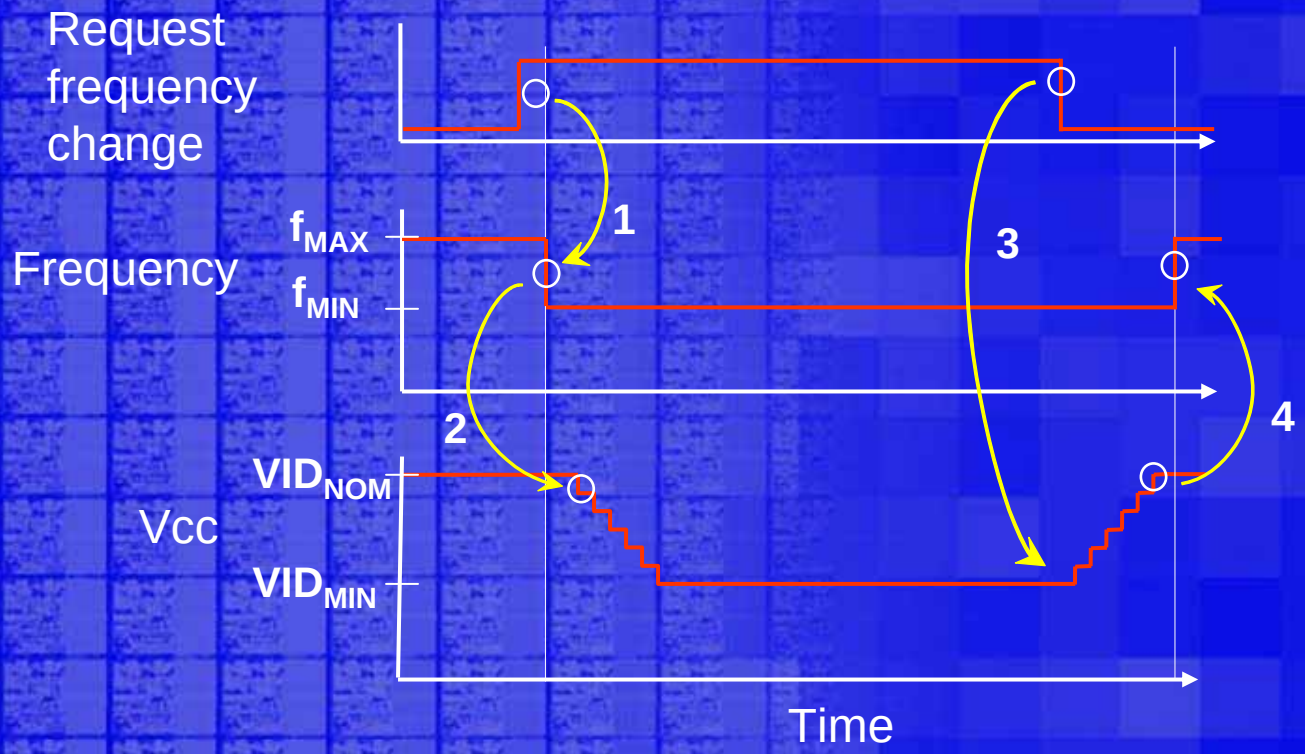
Thermal Management

- Dual core power dissipation
  - Power dissipation depends on software applications
  - Operating system determines application load balance
  - One core can be at maximum utilization while the other is idle
  - No relation between two cores in terms of power dissipation
- Thermal diodes used to monitor processor temperature



Dynamic Voltage IDentification (VID)



- Processor can change voltage and frequency at any time
  - Frequency is reduced before voltage is lowered
  - Requested voltage changes via Voltage IDentification (VID) pins
  - Voltage Regulator adjusts output accordingly
- Supported on all Desktop platforms

Enhanced Intel SpeedStep® Technology

- Same Intel SpeedStep® Technology for mobile processors but with a different focus
  - Mobile implements SpeedStep to extend battery life
  - DT and Server use it to save power and reduce fan speed
- Operating system monitors processor loading
  - Lower frequency selected when lightly loaded
  - Higher frequencies used as workload increases
  - ACPI manages the request by the OS to change frequency
- Supported on 6XX series and Pentium D processors for ratio multipliers greater than 14

Halt (C1) And Enhanced Halt (C1E) States

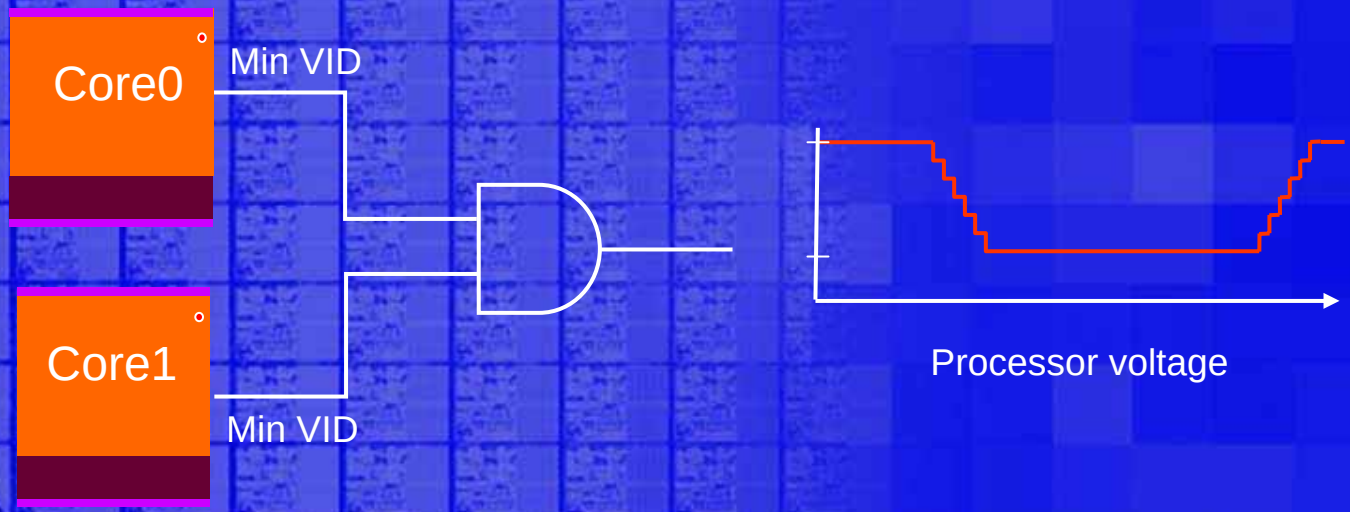
- Processor enters C1 whenever the Halt instruction is run
  - As frequent as in-between keystrokes (1st implemented on Windows* 3.1)
  - Very application dependent
  - C1 is also referred to as the Idle, Halt or Auto-Halt state
- C1 is a low power state
  - 90% of clocks are stopped, 10% still running at full speed
  - Exit halt state when interrupt is received
- C1E is C1 state but with a significant difference
  - Clock frequency is reduced to 2.8GHz (ratio multiplier of 14)
  - 90% of clocks are stopped, 10% still running at minimum speed
  - Processor voltage (VID) is also reduced
  - Result is a lower power state than C1 – about 10W savings

The Difference Between C1E and EIST

- Both use the same circuits within the processor
- But they are initiated in different ways
  - C1E happens whenever the Halt or MWait instruction is run
  - EIST when the OS requests a different performance level

Dual Core Voltage Restrictions

- Dual core processors have a single shared voltage plane
  - Both cores run off the same VR
  - Dynamic VID activity requires coordination between cores
- Both cores must be ready for a reduction in voltage
  - Cores communicate and request minimum voltage when both are ready
  - One cores frequency may drop but voltage reduction will wait for 2nd core



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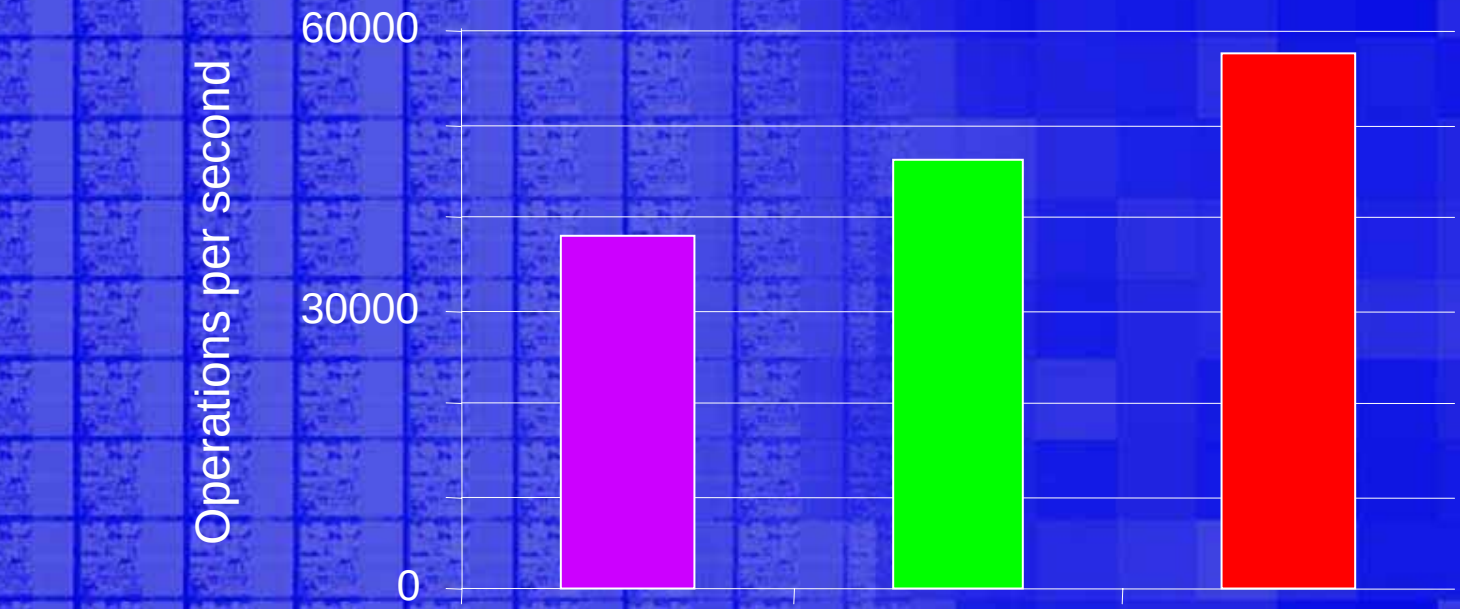
Performance Comparisons

Source: http://www.veritest.com/clients/reports/intel/intel_se7520af2_specjbb2000.pdf

Intel® Server Board SE7520AF2 with Intel® Xeon™ 3.6GHz 1M cache processor: SPECjbb2000 benchmark testing

Test report prepared under contract from Intel® Corporation



Single processor 3.6 GHz Intel Xeon 1M cache processor system with HT Enabled

Dual processor system with two 3.2 GHz Intel Xeon 1M cache processors with HT Disabled

Dual processor system with two 3.2 GHz Intel Xeon 1M cache processors with HT Enabled

SPECjbb is a trademark of the Standard Performance Evaluation Corp. (SPEC). SPECjbb2000 is an industry standard performance benchmark that measures the performance of servers running typical Java business applications.

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Summary

- Hyper-Threading Technology started the volume client transition to greater levels of parallelism
- Multi Core is the next step in the evolution of parallelism that provides 2 full execution cores in a single processor
- OS's and applications are already available to take advantage of parallelism
- Enhanced Intel Speedstep technology and C1E may reduce system power and fan noise

Applications and systems should be designed to take full advantage of the performance capabilities delivered by multi-core processors